

Claims

- [c1] A method for reducing shallow trench isolation (STI) consumption during semiconductor device processing, the method comprising:
- forming a hardmask over a semiconductor substrate;
 - patterning said hardmask and forming a trench within said substrate;
 - filling said trench with an insulative material;
 - implanting said insulative material with boron ions; and
 - annealing said insulative material.
- [c2] The method of claim 1, wherein said hardmask further comprises:
- a pad oxide material formed on said substrate; and
 - a pad nitride material formed on said pad oxide.
- [c3] The method of claim 1, further comprising recessing a portion of said insulative material prior to said implanting said insulative material.
- [c4] The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 1×10^{15} atoms/cm² to about 2×10^{16} atoms/cm².

- [c5] The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 3×10^{15} atoms/cm² to about 1×10^{16} atoms/cm².
- [c6] The method of claim 1, wherein said implanting said insulative material is carried out at a boron ion dose of about 6×10^{15} atoms/cm².
- [c7] The method of claim 1, further comprising forming a nitride liner within said trench prior to said filling said trench with an insulative material.
- [c8] The method of claim 1, further comprising forming a thermal oxide liner within said trench prior to said filling said trench with an insulative material.
- [c9] The method of claim 1, wherein said insulative material further comprises a high-density plasma oxide (HDP) material.
- [c10] A semiconductor device trench isolation structure, comprising:
a substrate having a trench region filled with an insulative material, wherein said insulative material is implanted with boron ions and thereafter annealed.
- [c11] The trench isolation structure of claim 10, wherein said boron ions implanted with a hardmask used in the for-

mation of said trench region, thereby self-aligning said boron ions to said trench region.

[c12] The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 1×10^{15} atoms/cm² to about 2×10^{16} atoms/cm².

[c13] The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 3×10^{15} atoms/cm² to about 1×10^{16} atoms/cm².

[c14] The trench isolation structure of claim 10, wherein said boron ions are implanted at a dose of about 6×10^{15} atoms/cm².

[c15] The trench isolation structure of claim 10, wherein said insulative material is formed over a nitride liner formed within said trench.

[c16] The trench isolation structure of claim 10, wherein said insulative material is formed over a thermal oxide liner formed within said trench.

[c17] The trench isolation structure of claim 10, wherein said insulative material further comprises a high-density plasma oxide (HDP) material.

[c18] A method for reducing the etch rate of an insulator layer, the method comprising:

implanting said insulative material with boron ions; and annealing said insulative material.

[c19] The method of claim 18, wherein said insulative material further comprises a silicon dioxide material.

[c20] The method of claim 18, wherein said insulative material further comprises a high-density plasma oxide (HDP) material.

[c21] The method of claim 20, wherein said implanting said insulative material is carried out at a boron ion dose of about 1×10^{15} atoms/cm² to about 2×10^{16} atoms/cm².

[c22] The method of claim 20, wherein said implanting said insulative material is carried out at a boron ion dose of about 3×10^{15} atoms/cm² to about 1×10^{16} atoms/cm².

[c23] The method of claim 20, wherein said implanting said insulative material is carried out at a boron ion dose of about 6×10^{15} atoms/cm².